CLAIMS

What is claimed is:

1. A method for envelope detection and extraction, said method including:

providing a first chopping signal derived from a first signal;

removing amplitude variation from the first signal without substantially disturbing a phase relationship between the first signal and the first chopping signal; and

multiplying the first signal with the first chopping signal to produce a first rectified signal and to upconvert in frequency a first direct current offset from mismatch corresponding to providing the first chopping signal, removing amplitude variation from the first signal, and multiplying the first signal.

2. The method of claim 1, further including filtering out the first direct current offset.

3. The method of claim 2, further including:

providing a second chopping signal derived from a second signal;

removing amplitude variation from the second signal without substantially disturbing a phase relationship between the second signal and the second chopping signal; and

multiplying the second signal with the second chopping signal to produce a second rectified signal and to upconvert in frequency a second direct current offset from mismatch corresponding to removing amplitude variation from the second signal, providing the second chopping signal, and multiplying the second signal.

4. The method of claim 3, further including filtering out the second direct current offset.

5. The method of claim 4, wherein multiplying the second signal includes converting the second signal from a voltage signal to a current signal.

6. The method of claim 5, further including comparing the first rectified signal with the second rectified signal to provide a difference signal, such that the difference signal includes a system direct current offset corresponding to a differential resistor.

7. The method of claim 3, further including delaying the second signal so that a difference in phase between the second chopping signal and the delayed second signal reduces substantially towards zero.

8. The method of claim 1, further including delaying the first signal so that a difference in phase between the first chopping signal and the delayed first signal reduces substantially towards zero.

9. The method of claim 1, wherein multiplying includes converting the first signal from a voltage signal to a current signal.

10. A system for envelope detection and extraction, the system including:

a first limiter configured to produce a first chopping signal from a first signal, wherein the first limiter is further configured to remove amplitude variation from the first signal without substantially disturbing a phase relationship between the first signal and the first chopping signal; and

a first mixer coupled to the first limiter, the first mixer configured to multiply the first signal with the first chopping signal to produce a first rectified signal and to upconvert in frequency a first direct current offset from mismatch corresponding to the first limiter and the first mixer.

11. The system of claim 10, further including an extractor element coupled to the first mixer, the extractor element configured to filter out the first direct current offset.

12. The system of claim 11, further including:

a second limiter configured to provide a second chopping signal derived from a second signal, wherein the second limiter is further configured to remove amplitude variation from a second signal without substantially disturbing a phase relationship between the second signal and the second chopping signal; and

a second mixer coupled to the second limiter, the second mixer configured to multiply the second signal with the second chopping signal to produce a second rectified signal and to upconvert in frequency a second direct current offset from mismatch corresponding to the second mixer and the second limiter.

13. The system of claim 12, wherein the extractor element is coupled to the second mixer, wherein the extractor element is further configured to filter out the second direct current offset.

14. The system of claim 13, wherein the second mixer is further configured to convert the second signal from a voltage signal to a current signal.

15. The system of claim 14, wherein the extractor element includes a differential resistor.

16. The system of claim 15, wherein the extractor element is configured to compare the first rectified signal with the second rectified signal to provide a difference signal across the differential resistor, such that the difference signal includes a system direct current offset corresponding to mismatch of the differential resistor.

17. The system of claim 12, further including a second delay element coupled to the second limiter and the second mixer, the second delay element configured to delay the second signal so that a difference in phase between the second chopping signal and the delayed second signal reduces substantially towards zero.

18. The system of claim 10, further including a second stage limiter coupled between at least one of the first limiter and the first mixer and a second limiter and a second mixer.

19. The system of claim 10, wherein the first mixer is further configured to convert the first signal from a voltage signal to a current signal.

20. The system of claim 10, wherein the first mixer includes a linear voltage-to-current element having at least one differential pair transistor, and a switching-core having differential pair transistors coupled to an output of the at least one differential pair transistor of the linear voltage-to-current element.

21. The system of claim 10, further including a second mixer and a second limiter configured substantially similar to the first mixer and the first limiter.

22. The system of claim 10, further including a first delay element coupled to the first limiter and the first mixer, the first delay element configured to delay the first signal so that a difference in phase between the first chopping signal and the delayed first signal reduces substantially towards zero.

23. The system of claim 10, wherein the first limiter is further configured to provide at least one of low AM-to-PM (amplitude modulation to phase modulation) distortion and sharp square-wave edges.

24. A system for envelope detection and extraction, the system including:

means for providing a chopping signal derived from a signal;

means for removing amplitude variation from the signal without substantially disturbing a phase relationship between the signal and the chopping signal; and

means for multiplying the signal with the chopping signal to produce a rectified signal and to upconvert in frequency a direct current offset from mismatch corresponding to the means for providing the chopping signal, the means for removing amplitude variation from the signal, and the means for multiplying the signal.

25. The system of claim 24, further including means for filtering out the direct current offset, such that a system direct current offset is primarily determined by a differential resistor included in the system.